



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,135	03/16/2004	Shunpei Yamazaki	12732-221001 / US7052	9241
26171 7590 05/30/2007 FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			EXAMINER SHAPIRO, LEONID	
			ART UNIT 2629	PAPER NUMBER
			MAIL DATE 05/30/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<p align="center">Office Action Summary</p>	<p>Application No.</p> <p align="center">10/801,135</p>	<p>Applicant(s)</p> <p align="center">YAMAZAKI ET AL.</p>	
	<p>Examiner</p> <p align="center">Leonid Shapiro</p>	<p>Art Unit</p> <p align="center">2629</p>	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-56 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 19-50 is/are rejected.
- 7) ☒ Claim(s) 13-18 and 51-56 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-12,27-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble (US 4,521,775) in view of Sera (JP 2001-068678 A).

As to claim 1, Noble teaches an integrated circuit device (see fig. 1, item 20) comprising:

a first display area (see fig. 1, item 16, col. 2, lines 10-21);

an integrated circuit including a plurality of semiconductor

films as a plurality of active region formed over an insulating film (see fig. 1, item 20);
and

a second display area that is formed over the first display area (see fig. 1, item 17, col. 2, lines 10-21) and connected to the thin film integrated circuit (see fig. 2, items 26-29, col. 2, lines 47-54).

Noble does not disclose a thin film integrated circuit.

Sera teaches a thin film integrated circuit (see Abstract).

It would have been obvious to one of ordinary skill in the art to incorporate teachings of Sera into Noble system in order to improve heat dissipation (see Problem to be solved in the Sera reference).

Art Unit: 2629

As to claim 2, Noble teaches an integrated circuit device (see fig. 1, item 20) comprising:

a first display area (see fig. 1, item 16, col. 2, lines 10-21);

an integrated circuit including a plurality of semiconductor films as a plurality of active region formed over an insulating film (see fig. 1, item 20); and

a second display area that is formed over the first display area (see fig. 1, item 17, col. 2, lines 10-21) and connected to the thin film integrated circuit (see fig. 2, items 26-29, col. 2, lines 47-54);

wherein display of the first display area is visible when the second display area is OFF (col. 1, lines 28-35).

Noble does not disclose a thin film integrated circuit.

Sera teaches a thin film integrated circuit (see Abstract).

It would have been obvious to one of ordinary skill in the art to incorporate teachings of Sera into Noble system in order to improve heat dissipation (see Problem to be solved in the Sera reference).

As to claims 3 Noble teaches an integrated circuit device (see fig. 1, item 20) comprising:

a first display area (see fig. 1, item 16, col. 2, lines 10-21);

an integrated circuit including a plurality of semiconductor films as a plurality of active region formed over an insulating film (see fig. 1, item 20); and

a second display area that is formed over the first display area (see fig. 1, item 17, col. 2, lines 10-21) and connected to the thin film integrated circuit (see fig. 2, items 26-29, col. 2, lines 47-54).

Noble does not disclose a thin film integrated circuit and a metal oxide provided over another surface of the insulating film.

Sera teaches a thin film integrated circuit (see Abstract) and insulation films made of a metal oxide (see Solution).

It would have been obvious to one of ordinary skill in the art to incorporate teachings of Sera into Noble system to provide a metal oxide over another surface of the insulating film in order to improve heat dissipation (see Problem to be solved in the Sera reference).

As to claim 4, Noble teaches an integrated circuit device (see fig. 1, item 20) comprising:

a first display area (see fig. 1, item 16, col. 2, lines 10-21);

an integrated circuit including a plurality of semiconductor films as a plurality of active region formed over an insulating film (see fig. 1, item 20);
and

a second display area that is formed over the first display area (see fig. 1, item 17, col. 2, lines 10-21) and connected to the thin film integrated circuit (see fig. 2, items 26-29, col. 2, lines 47-54);

wherein display of the first display area is visible when the second display area is OFF (col. 1, lines 28-35).

Noble does not disclose a thin film integrated circuit and a metal oxide provided over another surface of the insulating film.

Sera teaches a thin film integrated circuit (see Abstract) and insulation films made of a metal oxide (see Solution).

It would have been obvious to one of ordinary skill in the art to incorporate teachings of Sera into Noble system to provide a metal oxide over another surface of the insulating film in order to improve heat dissipation (see Problem to be solved in the Sera reference).

As to claims 5 Noble teaches an integrated circuit device (see fig. 1, item 20) comprising:

- a first display area (see fig. 1, item 16, col. 2, lines 10-21);

- an integrated circuit having a plurality of transistors formed over one surface of an insulating film (see fig. 1, item 20); and

- a second display area that is formed over the first display area (see fig. 1, item 17, col. 2, lines 10-21) and connected to the thin film integrated circuit (see fig. 2, items 26-29, col. 2, lines 47-54).

Noble does not disclose a thin film integrated circuit and a metal oxide provided over another surface of the insulating film.

Sera teaches a thin film integrated circuit (see Abstract) and insulation films made of a metal oxide (see Solution).

It would have been obvious to one of ordinary skill in the art to incorporate teachings of Sera into Noble system to provide a metal oxide over another surface of

Art Unit: 2629

the insulating film in order to improve heat dissipation (see Problem to be solved in the Sera reference).

As to claims 6 Noble teaches an integrated circuit device (see fig. 1, item 20) comprising:

a first display area (see fig. 1, item 16, col. 2, lines 10-21);

an integrated circuit having a plurality of transistors

formed over one surface of an insulating film (see fig. 1, item 20); and

a second display area that is formed over the first display area (see fig. 1, item 17, col. 2, lines 10-21) and connected to the thin film integrated circuit (see fig. 2, items 26-29, col. 2, lines 47-54);

wherein display of the first display area is visible when the second display area is OFF (col. 1, lines 28-35).

Noble does not disclose a thin film integrated circuit and a metal oxide provided over another surface of the insulating film.

Sera teaches a thin film integrated circuit (see Abstract) and insulation films made of a metal oxide (see Solution).

It would have been obvious to one of ordinary skill in the art to incorporate teachings of Sera into Noble system to provide a metal oxide over another surface of the insulating film in order to improve heat dissipation (see Problem to be solved in the Sera reference).

As to claims 27-32, Noble teaches the first display area and the second display area are similar in size (fig. 1, items 16-17).

As to claims 33-50, Noble teaches the first display area and the second display area are combined whereby displaying letters, graphics, symbols or the combination thereof, a static or moving image (fig. 1, lines 8-27).

2. Claims 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble and Sera as applied to claims 1-6 above, and further in view of Takahashi et al. (US 2005/0030404 A1).

Noble and Sera do not disclose the first display area is a photograph.

Takahashi et al. teaches display area is a photograph (paragraph 0047).

It would have been obvious to one of ordinary skill in the art to incorporate teachings of Takahashi et al. into Sera and Noble system in order to be overlapped (paragraph 0047 in the Takahashi et al. reference).

3. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble and Sera as applied to claims 1-6 above, and further in view of Yokono et al. (US 5,300,735).

Noble and Sera do not disclose metal film is formed from an element selected from the group consisting of W, Ti, Ta, Mo, Nd, Ni, Co, Zr, Zn, Ru, Rh, Pd, Os, and Ir, or an alloy material or a compound material which is based on the element; or an oxide of the metal compound.

Yokono et al. teaches metal film is formed from an element selected from the group consisting of Ni, Zn (col. 6, lines 21-49).

It would have been obvious to one of ordinary skill in the art to incorporate teachings of Yokono et al. into Sera and Noble system in order to improve reliability of devices having multilayer conductor films fabricated by thin-film technology, such as ICs (col. 49, lines 30-34 in the Yokono et al. reference).

4. Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble and Sera as applied to claims 1-6 above, and further in view of Yoshimura et al. (JP 60198861 A).

Noble and Sera do not disclose metal oxide is WO₂ or WO₃.

Yoshimura et al. teaches metal oxide is WO₃ (Constitution).

It would have been obvious to one of ordinary skill in the art to incorporate teachings of Yoshimura et al. into Sera and Noble system in order to increase ON-current (Purpose in the Yoshimura et al. reference).

Allowable Subject Matter

5. Claims 13-18, 51-56 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claims 13-18 the major difference between the teaching of the prior art of record (Noble, Sera and Takahashi et al.) and the instant invention a dual emission light-emitting device.

Relative to claims 51-56 the major difference between the teaching of the prior art of record (Noble, Sera and Takahashi et al.) and the instant invention is the thin film integrated circuit device is an IC card.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2629

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS
05.27.07



RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600